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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,005	06/14/2001	Michio Horiuchi	149-01	5592

7590 09/30/2003

Paul & Paul
2900 Two Thousand Market Street
Philadelphia, PA 19103

EXAMINER
OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,005	HORIUCHI ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *6-10, 17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 16, 2003 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 5, 11 – 13, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent No. 6,335,565 to Miyamoto et al.

Regarding claim 1, Miyamoto et al. teaches a multi-layered semiconductor device (Fig. 34) characterized in that a film-like package incorporating therein a semiconductor chip (AD, MF) is disposed in a package accommodation opening of a circuit pattern layer (Col. 27, lines 5 – 15; The etched copper foil forms a circuit pattern) to form a circuit board, said circuit pattern layer comprises a substrate, a circuit pattern formed on

the substrate, and said package accommodation opening and a plurality of such circuit boards are layered together to electrically connect the circuit patterns of the respective circuit boards with each other (Col. 6, lines 37 – 47). Furthermore, the circuit pattern layer of the opening for the chip is an inherent feature of the device, since the circuit pattern enables communication with the semiconductor chip.

Regarding claims 2 and 13, Miyamoto et al. teaches a multi-layered semiconductor device, wherein every adjacent circuit board is bonded to another with an insulation adhesive except for an electrically connected portion (Fig. 34 (10); Col. 22, lines 29 – 42; Col. 26, lines 38 – 39).

Regarding claims 3 and 16, Miyamoto et al. teaches a multi-layered semiconductor device, wherein the electrical connection between the circuit patterns on the respective circuit boards is performed via a low melting point metal filled in a through-hole (8a, 8b) formed in the semiconductor package (Fig. 35 (11); Col. 26, lines 41 –44).

Regarding claim 4, Miyamoto et al. teaches a multi-layered semiconductor device, wherein the electrical connection between the circuit patterns on the circuit boards is performed by connecting an extension of the circuit pattern into a hole formed in the semiconductor package with an electrode pad of the circuit pattern in the other board positioned beneath the formed board (Fig. 35, solder (11) connecting copper leads (5a) and bumps (9); Col. 27, lines 9 – 20).

Regarding claim 5, Miyamoto et al. teaches a multi-layered semiconductor device, wherein the electric connection between the semiconductor package and a

circuit pattern layer accommodating the semiconductor package is performed by connecting an extension of the circuit pattern, formed on the semiconductor package to project outside the package, with an electrode pad of the circuit pattern layer (Fig. 34, bump (9)).

Regarding claim 11, Miyamoto et al. teaches a multi-layered semiconductor device, as recited above, wherein the substrate is an insulation substrate (Col. 26, lines 33 and 34).

Regarding claim 12, Miyamoto et al. teaches a multi-layered semiconductor device, wherein at least one of the plurality of circuit boards incorporates a plurality of semiconductor chips (Col.6, lines 4 – 7).

Regarding claim 15, Miyamoto et al. teaches a multi-layered semiconductor device, wherein the electric connection between the semiconductor chip and the board is by flip-chip connection (Fig. 34. (4)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. as applied to claims 1 – 5 and 11 above, and further in view of US Patent No. 3,672,034 to Clark.

Miyamoto et al. teaches a multi-layered semiconductor device, wherein the semiconductor chip is accommodated in a through-hole formed in the insulation substrate of at least one of the plurality of circuit boards. Miyamoto et al. does not teach that the chip is electrically connected to the circuit of the circuit board by a beam lead bonding. Clark teaches using beam leads to connect a semiconductor device to a circuit (Col. 1, lines 20 – 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the beam lead taught by Clark into the device taught by Miyamoto et al., since it is desirable to reduce the cost of connecting the semiconductor device to the rest of the circuit.

Response to Arguments

6. Applicant's arguments filed July 9, 2003 have been fully considered but they are not persuasive.

With respect to arguments that Miyamoto et al. does not teach a circuit pattern, see Col. 27, lines 5 – 15. The etched copper foil forms a circuit pattern. Furthermore, the circuit pattern layer of the opening for the chip is an inherent feature of the device, since the circuit pattern enables communication with the semiconductor chip.

The Applicant argues that Miyamoto et al. does not teach a lead extending from the circuit, that is bonded, in a through-hole of the insulation substrate to a circuit on

another circuit board. This teaching is shown in Fig. 35 and Col. 26, lines 41 – 44, as explained above.

7. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

8. Applicant's arguments with respect to claim 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DWO

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800